A
(21119)

Roll No. .....

Total Questions : 13] [Printed Pages : 4

NP–3603

B.Sc. (Computer Science) IIIrd Semester Examination, Nov., 2019

SWITCHING THEORY AND LOGIC DESIGN

(BCS–302)

Time : 3 Hrs.] *[M.M. : 75*

Note :– Attempt all the Sections as per instructions.

Section–A

(Very Short Answer Type Questions) 3×5=15

Note :– Attempt all the *five* questions. Each question carries 3 marks.

1. Convert the following numbers to 8 bit 2's complement form :

   -57_{10}

2. Find 2's complement for the given binary number :

   (i) 101101

   (ii) 1011001

3. Reduce the Boolean expression :

$$Y = \bar{A}\bar{B}C + A\bar{B}\bar{C}$$

4. Simplify the expression :

$$Y = A(B + \bar{C}A) + (BC)(B + \bar{C}A)$$

5. Convert the following decimal numbers to excess 3 code :

   (i) 14

   (ii) 32

Section–B

(Short Answer Type Questions) 7½×2=15

Note :– Attempt any *two* questions out of the following three questions. Each question carries 7½ marks.

6. Define sequential circuits. What are the advantages of JK flip-flop over an SR flip-flop ?

7. Write down the comparison between combinational circuit and sequential logic circuit and what are the uses of asynchronous inputs of flip-flops.

8. Define a shift register and also draw the block diagram of parallel in serial out shift register and serial in parallel out shift register.

Section–C

(Long Answer Type Questions) 15×3=45

Note :– Attempt any *three* questions out of the following five questions. Each question carries 15 marks. Answer is required in detail.

9. An asynchronous sequential circuit is described by the following excitation and output functions :

$$y = x_1x_2 + (x_1 + x_2)y$$

$$z = y$$

(i) Draw the logic diagram.

(ii) Derive transition table and output map.

10. Write short notes on the following :

(i) Fault detection methods

(ii) TTL and CMOS tri-state logic

(iii) Race free state assignment

11. (a) Convert the D flip-flop using JK flip-flop.

(b) Write down the difference between multiplexer and a demultiplexer.

12. Implement the following function

$$F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 7, 8, 9, 11, 14, 15)$$

using :

(i) 8 : 1 MUX

(ii) 4 : 1 MUX

(iii) 2 : 1 MUX

13. (a) Design 5 to 32 decorder using one 2 to 4 and four 3 to 8 decorders.

(b) Design a full adder using ROM.