Additional Exercises

Question 14.12:

The number of silicon atoms per m^3 is 5×10^{28}. This is doped simultaneously with 5×10^{22} atoms per m^3 of Arsenic and 5×10^{20} per m^3 atoms of Indium. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16}\ m^{-3}$. Is the material n-type or p-type?

Answer

Number of silicon atoms, $N = 5 \times 10^{28}$ atoms/m^3

Number of arsenic atoms, $n_{As} = 5 \times 10^{22}$ atoms/m^3

Number of indium atoms, $n_{In} = 5 \times 10^{20}$ atoms/m^3

Number of thermally-generated electrons, $n_i = 1.5 \times 10^{16}$ electrons/m^3

Number of electrons, $n_e = 5 \times 10^{22} - 1.5 \times 10^{16} \approx 4.99 \times 10^{22}$

Number of holes = n_h

In thermal equilibrium, the concentrations of electrons and holes in a semiconductor are related as: $n_e n_h = n_{i2}$

$$\therefore n_h = \frac{n_i^2}{n_e}$$

$$= \frac{\left(1.5 \times 10^{16}\right)^2}{4.99 \times 10^{22}} \approx 4.51 \times 10^{9}$$

Therefore, the number of electrons is approximately 4.99×10^{22} and the number of holes is about 4.51×10^{9}. Since the number of electrons is more than the number of holes, the material is an n-type semiconductor.

Question 14.13:

In an intrinsic semiconductor the energy gap E_g is 1.2 eV. Its hole mobility is much smaller than electron mobility and independent of temperature. What is the ratio between

conductivity at 600K and that at 300K? Assume that the temperature dependence of intrinsic carrier concentration n_i is given by

$$n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$$

where n_0 is a constant.

Answer

Energy gap of the given intrinsic semiconductor, E_g = 1.2 eV

The temperature dependence of the intrinsic carrier-concentration is written as:

$$n_i = n_0 \exp\left[-\frac{E_g}{2k_B T}\right]$$

Where, k_B = Boltzmann constant = 8.62 × 10^{-5} eV/K T = Temperature n_0 = Constant

Initial temperature, T_1 = 300 K

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i1} = n_0 \exp\left[-\frac{E_g}{2k_B \times 300}\right] \ldots (1)$$

Final temperature, T_2 = 600 K

The intrinsic carrier-concentration at this temperature can be written as:

$$n_{i2} = n_0 \exp\left[-\frac{E_g}{2k_B \times 600}\right] \ldots (2)$$

The ratio between the conductivities at 600 K and at 300 K is equal to the ratio between the respective intrinsic carrier-concentrations at these temperatures.

$$\frac{n_{i2}}{n_{i1}} = \frac{n_0 \exp\left[-\frac{E_g}{2k_B 600}\right]}{n_0 \exp\left[-\frac{E_g}{2k_B 300}\right]}$$

$$= \exp\frac{E_g}{2k_B}\left[\frac{1}{300} - \frac{1}{600}\right] = \exp\left[\frac{1.2}{2 \times 8.62 \times 10^{-5}} \times \frac{2-1}{600}\right]$$

$$= \exp[11.6] = 1.09 \times 10^5$$

Therefore, the ratio between the conductivities is 1.09×10^5.

Question 14.14:

In a p-n junction diode, the current I can be expressed as

$$I = I_0 \exp\left(\frac{eV}{2k_B T} - 1\right)$$

where I_0 is called the reverse saturation current, V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, $k_B$is the Boltzmann constant (8.6×10^{-5} eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and T = 300 K, then

(a) What will be the forward current at a forward voltage of 0.6 V?

(b) What will be the increase in the current if the voltage across the diode is increased to 0.7 V?

(c) What is the dynamic resistance?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V? Answer

In a p-n junction diode, the expression for current is given as:

$$I = I_0 \exp\left(\frac{eV}{2k_B T} - 1\right)$$

Where,

I_0 = Reverse saturation current = 5×10^{-12} A

T = Absolute temperature = 300 K

k_B = Boltzmann constant = 8.6×10^{-5} eV/K = 1.376×10^{-23} J K^{-1}

V = Voltage across the diode

(a) Forward voltage, V = 0.6 V

$$\therefore \text{Current, } I = 5 \times 10^{-12}\left[\exp\left(\frac{1.6 \times 10^{-19} \times 0.6}{1.376 \times 10^{-23} \times 300}\right) - 1\right]$$

$$= 5 \times 10^{-12} \times \exp[22.36] = 0.0256 \text{ A}$$

Therefore, the forward current is about 0.0256 A.

(b) For forward voltage, V′ = 0.7 V, we can write:

$$I' = 5 \times 10^{-12}\left[\exp\left(\frac{1.6 \times 10^{-19} \times 0.7}{1.376 \times 10^{-23} \times 300} - 1\right)\right]$$

$$= 5 \times 10^{-12} \times \exp[26.25] = 1.257 \text{ A}$$

Hence, the increase in current, $\Delta I = I' - I$

= 1.257 − 0.0256 = 1.23 A

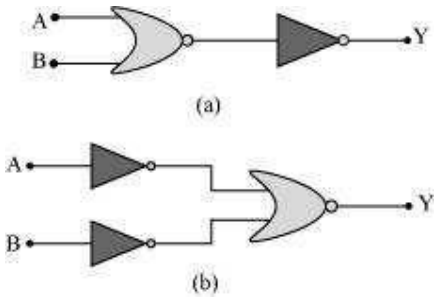
(c) Dynamic resistance $= \frac{\text{Change in voltage}}{\text{Change in current}}$

$$= \frac{0.7 - 0.6}{1.23} = \frac{0.1}{1.23} = 0.081\ \Omega$$

(d) If the reverse bias voltage changes from 1 V to 2 V, then the current (I) will almost remain equal to I_0 in both cases. Therefore, the dynamic resistance in the reverse bias will be infinite.

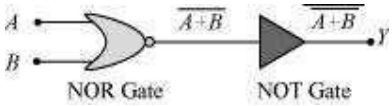
Question 14.15:

You are given the two circuits as shown in Fig. 14.44. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.



Answer

(a) A and B are the inputs and Y is the output of the given circuit. The left half of the given figure acts as the NOR Gate, while the right half acts as the NOT Gate. This is shown in the following figure.



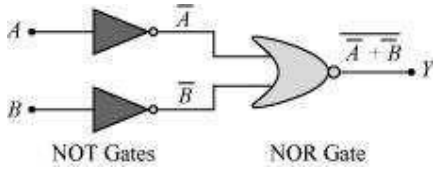
Hence, the output of the NOR Gate = $\overline{A+B}$

This will be the input for the NOT Gate. Its output will be $\overline{\overline{A+B}}$ = A + B

∴Y = A + B

Hence, this circuit functions as an OR Gate.

(b) A and B are the inputs and Y is the output of the given circuit. It can be observed from the following figure that the inputs of the right half NOR Gate are the outputs of the two NOT Gates.



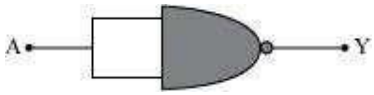
Hence, the output of the given circuit can be written as:

$Y = \overline{\overline{A}+\overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$

Hence, this circuit functions as an AND Gate.

Question 14.16:

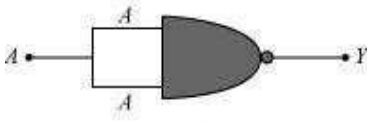
Write the truth table for a NAND gate connected as given in Fig. 14.45.



Hence identify the exact logic operation carried out by this circuit.

Answer

A acts as the two inputs of the NAND gate and Y is the output, as shown in the following figure.



NAND Gate

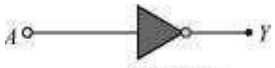
Hence, the output can be written as:

$$Y = \overline{A \cdot A} = \bar{A} + \bar{A} = \bar{A} \quad \ldots (i)$$

The truth table for equation (i) can be drawn as:

A	Y $(=\bar{A})$
0	1
1	0

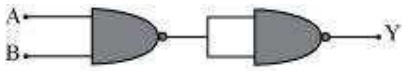
This circuit functions as a NOT gate. The symbol for this logic circuit is shown as:



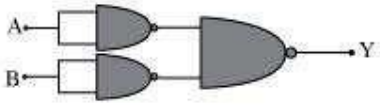
NOT Gate

Question 14.17:

You are given two circuits as shown in Fig. 14.46, which consist of NAND gates. Identify the logic operation carried out by the two circuits.



(a)

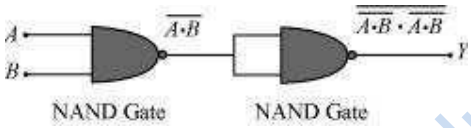


(b)

Answer

In both the given circuits, A and B are the inputs and Y is the output.

(a) The output of the left NAND gate will be $\overline{A.B}$, as shown in the following figure.

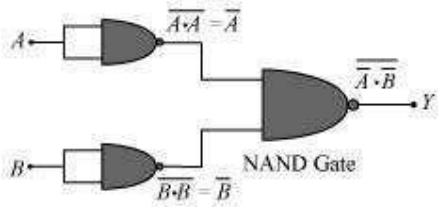


Hence, the output of the combination of the two NAND gates is given as:

$$Y = \overline{\left(\overline{A \cdot B}\right) \cdot \left(\overline{A \cdot B}\right)} = \overline{\overline{AB}} + \overline{\overline{AB}} = AB$$

Hence, this circuit functions as an AND gate.

(b) $\overline{A}$ is the output of the upper left of the NAND gate and $\overline{B}$ is the output of the lower half of the NAND gate, as shown in the following figure.



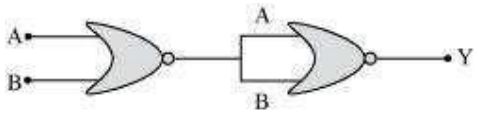
Hence, the output of the combination of the NAND gates will be given as:

$$Y = \overline{A} \cdot \overline{B} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

Hence, this circuit functions as an OR gate.

Question 14.18:

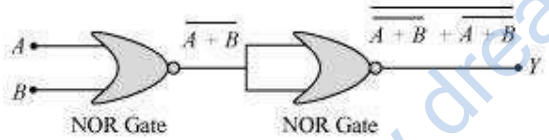
Write the truth table for circuit given in Fig. 14.47 below consisting of NOR gates and identify the logic operation (OR, AND, NOT) which this circuit is performing.



(Hint: A = 0, B = 1 then A and B inputs of second NOR gate will be 0 and hence Y=1. Similarly work out the values of Y for other combinations of A and B. Compare with the truth table of OR, AND, NOT gates and find the correct one.)

Answer

A and B are the inputs of the given circuit. The output of the first NOR gate is $\overline{A+B}$. It can be observed from the following figure that the inputs of the second NOR gate become the out put of the first one.



Hence, the output of the combination is given as:

$$Y = \overline{\overline{A+B} + \overline{A+B}} = \overline{\overline{A}\cdot\overline{B}} + \overline{\overline{A}.\overline{B}}$$

$$= \overline{\overline{A}\cdot\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$$

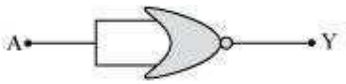
The truth table for this operation is given as:

A	B	Y (=A + B)
0	0	0
0	1	1
1	0	1
1	1	1

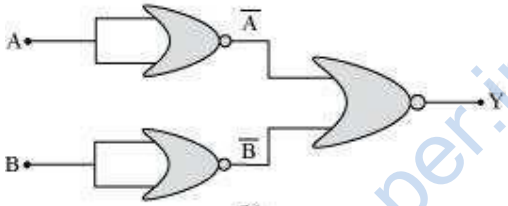
This is the truth table of an OR gate. Hence, this circuit functions as an OR gate.

Question 14.19:

Write the truth table for the circuits given in Fig. 14.48 consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.



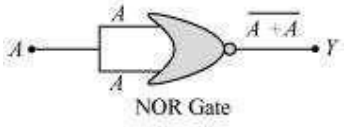
(a)



(b)

Answer

(a) A acts as the two inputs of the NOR gate and Y is the output, as shown in the following figure. Hence, the output of the circuit is $\overline{A + A}$.

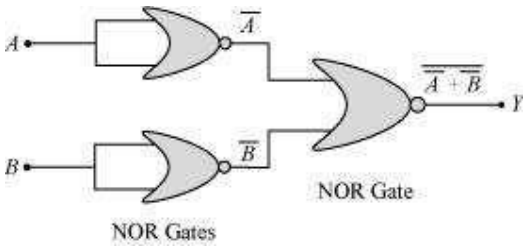


Output, $Y = \overline{A + A} = \overline{A}$

The truth table for the same is given as:

A	Y $\left(=\overline{A}\right)$
0	1
1	0

This is the truth table of a NOT gate. Hence, this circuit functions as a NOT gate. (b) A and B are the inputs and Y is the output of the given circuit. By using the result obtained in solution (a), we can infer that the outputs of the first two NOR gates are $\overline{A}$ and $\overline{B}$, as shown in the following figure.



$\overline{A}$ and $\overline{B}$ are the inputs for the last NOR gate.

Hence, the output for the circuit can be written as:

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

The truth table for the same can be written as:

A	B	Y (=A!B)
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table of an AND gate. Hence, this circuit functions as an AND gate.